hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instruction[s], and

software means responding to an indication that a memory address to be written stores a target instruction which has been translated to at least one host instruction[s] for [protecting against writing the memory address until it has been assured] assuring that host instructions translated from target instructions stored at [translations associated with] the memory address will not be utilized [before being updated] once the memory address has been written.

Claim 2 (amended). A system for [protecting memory from being written] maintaining translation consistency as claimed in Claim 1 in which the hardware means comprises:

a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and

a storage position in each storage location of the translation look aside buffer.

Claim 3 (amended). A system for [protecting memory from being written] maintaining translation consistency as claimed in Claim 1 in which the software means [for protecting against writing the memory address] invalidates [translations associated with] host instructions translated from target instructions stored at the memory address.

Cancel Claim 4.

Claim 4 (amended). A system for [protecting memory from being written] maintaining translation consistency as claimed in Claim 1 in which the software means for protecting against writing the memory address removes translations associated with the memory address.

Claim 5 (amended). A system for [protecting memory from being written] maintaining translation consistency as claimed in Claim 1 in which the hardware means comprises:

a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and

a storage position in each storage location of the translation look aside buffer; and

in which the software means for protecting against writing the memory address removes translations associated with the memory address.

Cancel Claims 10, 11, 14-17.

Claim 18, line 11, change "beforeaccessing" to --before accessing--.

Claim 12 (amended). A memory controller as claimed in Claim 11 in which the means for detecting an indication in a storage location to prevent a write access of [to] the physical address and for indicating a subsequent operation before accessing the address comprises

means for generating an exception in response to detection of an indication, and